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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/039,344	03/13/98	KIMSAL	C 16468

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EXAMINER

NGUYEN, M

ART UNIT

PAPER NUMBER

2816

DATE MAILED 3/99

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

## Office Action Summary

Application No. <b>09/039,344</b>	Applicant(s) <b>Kimsal et al.</b>
Examiner <b>Minh Nguyen</b>	Group Art Unit <b>2816</b>

Responsive to communication(s) filed on Sep 28, 1999

This action is **FINAL**.

Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

### Disposition of Claims

Claim(s) 1-16 and 18-22 is/are pending in the application.

Of the above, claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

Claim(s) \_\_\_\_\_ is/are allowed.

Claim(s) 1, 2, 4-9, 11-16, and 19-22 is/are rejected.

Claim(s) 3, 10, and 18 is/are objected to.

Claims \_\_\_\_\_ are subject to restriction or election requirement.

### Application Papers

See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.

The proposed drawing correction, filed on \_\_\_\_\_ is  approved  disapproved.

The specification is objected to by the Examiner.

The oath or declaration is objected to by the Examiner.

### Priority under 35 U.S.C. § 119

Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

All  Some\*  None of the CERTIFIED copies of the priority documents have been

received.

received in Application No. (Series Code/Serial Number) \_\_\_\_\_.

received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\*Certified copies not received: \_\_\_\_\_.

Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

### Attachment(s)

Notice of References Cited, PTO-892

Information Disclosure Statement(s), PTO-1449, Paper No(s). 3 and 9

Interview Summary, PTO-413

Notice of Draftsperson's Patent Drawing Review, PTO-948

Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

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## **DETAILED ACTION**

1. Applicants' amendment filed on 9/28/99 has been received and entered in the case. The amendments and arguments presented therein overcome the indefiniteness rejections and informality objections, however, the prior art rejection is maintained, as set forth below. This action is **FINAL**.
2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

### ***Claim Objections***

3. Claim 1 and 9 are objected to because of the following informalities:  
In claim 1, line 4, --input-- should be inserted after "first", second occurrence.  
In claim 9, line 7, --,-- should be inserted after "circuit".

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

4. Claims 1, 2, 4, 5, 8, 9, 11, 12, 14-16, 20, 21 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Colli et al. (U.S. Patent No. 5,825,218).

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As per claims 1, 20 and 22, Colli et al. discloses a linear ramp generating circuit (Fig. 5) comprising: an output node Vout, a first input node (input to switch Sw2) coupled to a first input signal COM; a second input node (input to switch Sw1) coupled to a second input signal (the inverted COM signal); a constant current source network (current sources 22 and 24); a capacitor C which has a first node coupled to ground, a second node coupled to Vout; a return charge network (transistors Q1a, Q1b, Q2a and Q2b, i.e., current source 20, comparator 28, FETs M1, M2 and M3), the return charge network is seen as analog active feedback circuit because it includes analog active components, i.e., bipolar transistors and FETs, comparator 28; a first switch means Sw2 responsive to the first input signal COM to discharge (switch Sw2 is opened) the capacitor C through the current source 22 and uncoupling (switch Sw2 is closed) the second node of the capacitor from the constant current source network; and a second switch means Sw1 responsive to the second input signal to charge the capacitor C through current source 20.

As per claim 2, the return charge network charges the capacitor through the current source 20 when switch Sw1 is closed.

As per claims 4, 15 and 21, the recited “FET pair” is seen as M1 and M2 and “op-amp” is seen as comparator 28.

As per claim 5, Colli et al clearly discloses the first node of the capacitor is ground.

As per claims 8 and 14, the return charge network is seen as active feedback circuit because it includes active components, i.e., bipolar transistors and FETs, the op-amp is seen as

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comparator 28, and the impedance feedback network is seen as the dynamic resistances of FETs M1, M2 and M3.

As per claim 9, the first node of the recharge network is the node which is created by the intersection of the collector terminal of transistor Q4a and the second node of the capacitor, and the second node of the recharge network is at the collector of transistor Q1b.

As per claim 11, the current source 22 is the current sink for the capacitor C because it provides the discharge path for the capacitor.

As per claim 12, this claim is rejected for the same reason as discussed above with regard to claim 5.

As per claim 16, this claim is rejected for the same reason as discussed above with regard to claim 1, and further, the current steering element is seen as switches Sw1 and Sw2.

#### *Claim Rejections - 35 USC § 103*

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Colli et al (U.S. Patent No. 5,825,218).

Colli et al discloses a linear ramp generation circuit as discussed above with regard to claim 1.

Not disclosed is that the constant current source is implemented using an op-amp. However, it is old and well-known in the art that constant current source can be implemented using an op-amp, of which fact official notice is taken. Moreover, an op-amp and op-amp circuit

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is well-known in electronic circuits for its high input impedance and low output impedance characteristics. It would have been obvious to one skilled in the art at the time of the invention to implement the constant current source of Colli et al using an op-amp so that the constant current source can be easily adapted to the rest of the ramp generator circuit due to its high input impedance and low output impedance characteristics.

6. Claims 7, 13 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Colli et al (U.S. Patent No. 5,825,218) in view of Diller (US Patent No. 4,728,813).

Colli et al. discloses the use of the first Sw2 and second Sw1 switches to control the time to discharge and recharge the capacitor via the input signals.

Not disclosed is that the first and second switches are implemented using differential paired transistors. Diller discloses first and second switches in a ramp generating circuit (Fig. 1) which can be implemented using differential paired transistors. It would have been obvious to one skilled in the art at the time of the invention to implement the first and second switches in Colli et al. circuit using differential paired transistors as taught by Diller because the switches which are implemented using differential paired transistors have the well-known advantage that both transistors will not both ON at the same time when receiving an input signal and its inversion to its input terminals of the differential pair.

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***Response to Arguments***

7. Applicant's arguments filed 9/28/99 have been fully considered but they are not persuasive.

Regarding the argument that the Colli reference does not disclose "the feature of an analog active feedback circuit", the examiner notes that the analog active feedback circuit reads on the comparator 28, the inverter which has its output connected to transistor M4 and transistor M4.

Regarding the argument that Colli et al does not disclose a hold period as recited in claim 20, the examiner notes that the hold period in the Colli reference circuit is the period of time when the switch Sw1 is closed and the capacitor is fully charged and before the switch Sw2 is still opened.

***Allowable Subject Matter***

8. Claims 3, 10 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3, 10 and 18 are allowable because the prior art of record fails to disclose or suggest a linear ramp generating circuit which includes an active feedback circuit in the return charge network wherein the active feedback circuit in the return charge network implements an approximately second order voltage response to the capacitor during the recovery mode of operation.

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***Conclusion***

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

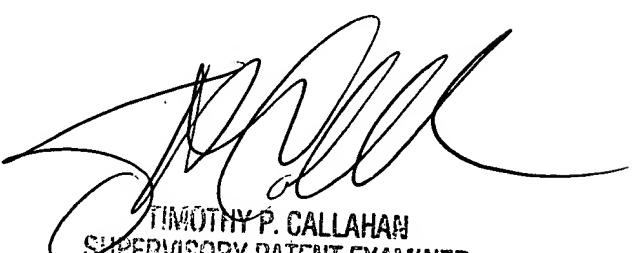
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is (703) 306-9179. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan, can be reached on (703)308-4876. The fax phone number for this Art Unit is (703)308-7722. Please note, any faxed paper clearly stating DRAFT or PROPOSED AMENDMENT at the top will be forwarded directly to the examiner. All others will be treated as a formal response and acted upon accordingly.

*MN*  
MN

November 1, 1999

  
TIMOTHY P. CALLAHAN  
SUPERVISORY PATENT EXAMINER  
GROUP 2500